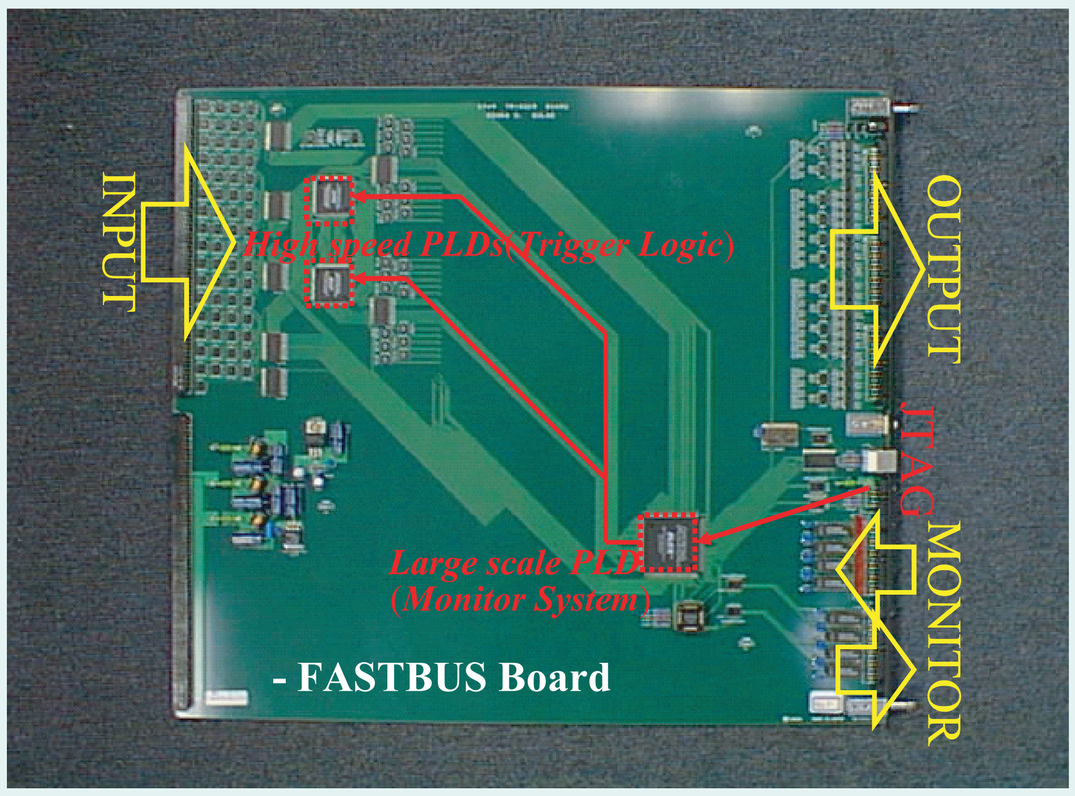
- *Programmable Level-0 Trigger Board*

The L0 trigger board for E787 used wire-wrap ECL logic in a FASTBUS board; one has to re-wire the board to modify the trigger condition. In E949, trigger modifications were expected because of the detector upgrade, and we therefore developed a new programmable L0 trigger board. The L0 trigger board has PLD chips (a product of ALTERA cooperation). Any trigger logic can be programmed using the Hardware Description Language(HDL). The PLD has In System Program(ISP) capability. The trigger conditions can be modified through JTAG link without extracting the board from the crate.



High-Speed PLD	EPM7032B-4
Large-Speed PLD	EPF10K100E-1
Board Size	FASTBUS
Input	65 ECL at back 16 ECL at front
Output	24 ECL(duplicated) 3 Or-ed 16 ECL at front

FIG. 3. A picture of the new L0 trigger board. Two high-speed PLD chips for trigger logic are located at top-left corner. A large-scale PLD chips for various applications is located at bottom-right corner.

The large-scale PLD was used for various applications.

- prescaler
- scaler
- hit pattern finder

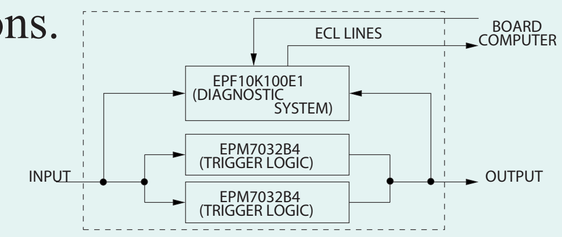


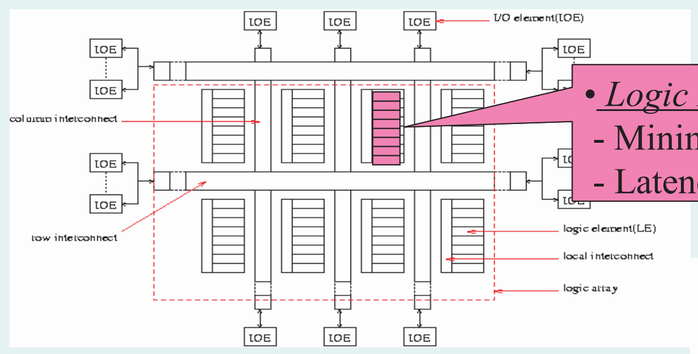
FIG. 4. A block diagram of the diagnostic system. The information is read through ECL lines from a computer.

The propagation time of the new board is required to be less than 19nsec for further trigger processing. The high-speed PLD and ECL/TTL converter chips meet the requirement.

ECL/TTL + TTL/ECL conversion	2nsec
EPM7032B-4	12nsec
Propagation on board	2nsec
TOTAL	16nsec

- *Digital Mean-timer in PLD*

A gate array has been used as a digital Mean-timer up to now. CPLDs are remarkably high-speed today and we therefore have developed a digital Mean-timer using CPLD.



- Hardware Description Language(HDL).
- Download through JTAG link.

Digital Mean-timer logic

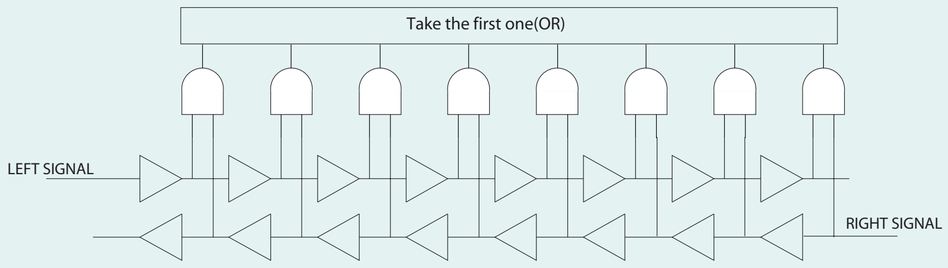


FIG. 5. Logic circuit of the digital Mean-timer described in HDL. The triangles represent a logic element which is the minimum component of the PLD(called ‘delay-cell’). The serial line of the delay-cells is called ‘delay-line’, and two delay-lines are used in the digital Mean-timer.

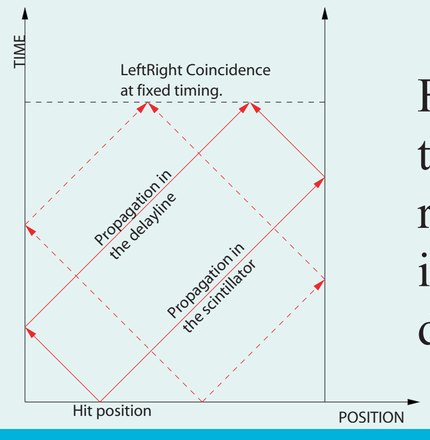


Fig. 6. Time progress of the signals in the scintillator and delay-line. Left-right coincidence for any hit positions in the scintillator (e.g. solid line and dashed line) occurs at the fixed timing.